Implementation of Novel Bridged-Insert Cascaded Five Level Inverter Topology Optimized With Enhanced EPSO Algorithm for commercial applications

SenthilKumar Arumugam 1, Alex George2, Sathish Kumar Shanmugam3, Karthikeyan Muthusamy4, Anbarasu Loganathan5

1Chettinad College of Engineering and Technology, Karaikudi, Tamilnadu, India.
2Sri Raganathar Institute of Engineering and Technology, Coimbatore, Tamilnadu, India.
3Jansons Institute of Technology, Coimbatore, Tamilnadu, India.
4Kongu Engineering College, Erode, Tamilnadu, India.
5Erode Sengunthar Engineering college, Erode, Tamilnadu, India.

Corresponding author

E-mail:1 bask2k1@yahoo.co.in, 2 vijayakumargovind@yahoo.co.in, 3 ssjjit.ac.in, 4 karthiadc@gmail.com, 5 lanbarasu78@yahoo.co.in

ABSTRACT

Inverters are basically power electronics devices that are used to convert DC power to AC at a required frequency and voltage level. Their main application area in real-time is in high voltage and high power applications in which cost of switching stress as well as total harmonic distortion must be low. Multilevel inverter technology has been emerging in recent times, as a very important structure in high power applications. Multi-level inverters also have a major role in interconnected grid systems used nowadays. There are several major topologies of multilevel inverters that exist in literature: Diode clamped (DMLI) (aka neutral-point clamped), Flying capacitor multilevel inverter (FCMLI) (aka capacitor-clamped) [6] and Cascaded H-bridges converter (CMLI) (i.e., cascaded multicell using separate dc sources). This paper discusses the principal benefits and drawbacks of increasing the number of levels of the inverter and how it has an effect on the efficiency and losses in the MLI architecture and how this difficulty as well as the overall performance of the systems can be improved using a novel Bridged-Cascaded H-bridge MLI topology. Proposed Methodology by EPSO algorithm (Enhanced particle swarm algorithm) helps the architecture more optimistic in harmonic reduction one also helps us to improve the efficiency. The system is an effective replacement for the conventional method which has high switching losses and eliminates the use of transformer. The simulation result portrays the effective control in the switching angle to obtain minimum THD performance, proposed design reduces the voltage oscillations by adapting the capacitor as auxiliary circuit and n-level inverter topologies possible. The paper proposes a novel bridged-insert cascaded MLI topology. The focus of the paper is on 5-level inverter topologies. The simulation has been carried out using MATLAB/Simulink, Tests with this crane and control system showed that residual vibration can be reduced by an order of magnitude and can remain insensitive to large changes in payload location in the vertical direction.

Keywords: MLI, oscillations, Simulation, THD.

1. INTRODUCTION

Power electronics involves the controlling and conditioning of electric power. The electric power maybe AC or DC power of given amplitude. Electric power conversion becomes necessary when the power handling capability of the load is different from what is actually available (at the input side or source end). The conversion is primarily done using switches- including semiconductor devices such as diodes, thyristors, IGBT’s, MOSFETS, etc [2],[3]. With advancements in technology, the demand for high power devices is on the rise. The power requirement these days are in the megawatt level. It is not possible nowadays to connect a single power semiconductor switch directly to a medium-voltage grid. The medium voltage grid has voltage ratings as follows: 2.3, 3.3, 4.16, or 6.9 kV. In order to overcome this problem, multilevel inverters have been invented [1]. Multilevel inverters are power electronic devices used to synthesize a required output voltage level from several input dc inputs voltage levels [4]. Multilevel inverters consist of an array of power semiconductor devices and other active elements such as capacitor. The commutation of the switches adds to the capacitor voltages. The power semiconductors however can withstand only reduced voltages [1]. Compared to conventional two-level inverter topologies, the multilevel inverter architectures provide a medium to high voltage range. Multilevel inverters provide enhanced voltage and current waveforms and also have the capability to reduce the unwanted harmonics. Multilevel inverters help diminish the switching losses. Their outputs yield multi-step voltage which helps to achieve improved power quality as well as better voltage capability. Of this, the most attractive feature is the small voltage step size of the multilevel inverters – it helps in achieving high voltage capability, lower harmonic components, lower switching losses, better electromagnetic compatibility, and improved power quality. The multilevel inverter can be functioned in both its fundamental as well as high switching frequencies [4].

The following are the advantages of multilevel inverter architecture:

a. It is the smaller output voltage step of multilevel inverters that is the main attractive feature [1], [4]:
   a. Increases the voltage capability
   b. Reduces the harmonic components present in the waveform
Besides the various advantages presented by a multilevel inverter, it also comes at the cost of a few disadvantages [4]:

1. The most notable drawback is that the power semiconductor switches require multilevel power conversion.
2. The small voltage steps are typically produced by isolated voltage sources or a bank of series capacitors. As for the isolated voltage sources their availability may be a major concern and the next problem is the voltage balance requirement of the series capacitor network.

II. LITERATURE SURVEY

Fig. 1, 2 and 3 depict one phase leg of inverters with different 2 levels, 3 levels and n levels, respectively [1]. An ideal switch can be used to represent a semiconductor device with x number of positions. The 2-level inverter generates an output voltage with two values with respect to the negative terminal of the capacitor, hence the name. Similarly, a 3-level inverter generates three voltages, and an n-level, n voltage values [1], [2],[3].
By varying the number of levels in the inverter, the output voltage will show varying number of steps. So, as the number of levels increase, the number of steps in the waveform will also correspondingly increase; it therefore reduces the harmonic distortion. But, on the other hand, as the number of levels is increased it leads to a rise in the complexity of the topology and also presents voltage imbalances [1]. The Capacitor model H-bridge Multilevel Inverter (CPHMLI) based modulation algorithm anticipated to eradicate the voltage oscillation for variable phase voltage source inverter circuits as shown in figure 4. The objective is to reduce the number of switching commutations to have total control over the voltage swings. The amplitude of the low-frequency switching voltage oscillations increases under certain nonlinear loads. So that the situation causes the system becomes unstable due to voltage variations. The proposed topology based control strategies able to control the switching voltage oscillations than previous converters and n-level diode-clamped converters. So that the situation causes the system becomes unstable due to voltage variations. The proposed topology based control strategies able to control the switching voltage oscillations than previous converters and n-level diode-clamped converters.

The proposed inverter topology ultimately controls the voltage, thus removing the low-frequency switching voltage oscillations of multiphase converters under any unbalanced and nonlinear loads. Fig. 4 below depicts a three-phase voltage source inverter, also known as a two-level inverter. P1, P2, and P3 are the poles and O is the neutral point. The poles are connected to loads and these loads are considered to be inductive. The current through an inductive circuit should never be open. So, a path should always be provided for the current to flow through. So, one of the ends of the pole is connected to the load terminal, whereas the other end will be connected to one throw or the other. Hence, a path will always be present for the current to pass through. Power can flow in both the directions. The switches can be depicted by IGBTs. We are using two IGBTs in a single leg. A single unit or switch is able to conduct current in both the directions. When one of the switches in a leg is on, the other is blocked or in OFF state [5], [6],[7].

A. REALIZATION OF DIFFERENT TYPES OF SWITCHES and vibrations

The damped-oscillation controller was first demonstrated using a suspended pay load having a natural frequency of 0.135 Hz. The demonstration used an ~14-m-long pendulum, and moves of several meters in 2 dof were attempted. Top speeds of \( \pm 1 \) m/s were obtained. Comparing typical runs with and without the damped-oscillation controller showed residual vibrations being reducing from \( \pm 30 \) cm to \( \pm 3 \) cm (an order of magnitude reduction). Note that this violation is equivalent to \( \pm 2 \times 10^3 \) rads. This is twice what was predicted in Fig. 3b (= 1 \( \times 10^3 \) rads) and is a result of nonlinear friction, imperfect drive wheels and bearing, and measurement inaccuracy present in the real system.

a. SPDT Switch or a simple 2-level inverter realization

The internal realization of simple SPDT switch using IGBTs and diodes is shown in Fig. 5 below. \( P^n \) represents the pole and T1 and T2, the throws. The voltage across the two throws is \( +V_{\text{DC}} \). One end of the pole will be connected to one of the throws (T1 or T2), and the other end to the load. Depending on the direction in which the load current is flowing through the switch, it is either the diode or the transistor that forms a component part of the switch that will be conducting. So, the diode and the transistor form a complementary pair (either S1 and D2 are ON or D1 and S2 are ON). The circuit therefore operates as a SPDT switch. There are only two possible output voltage levels at the pole end: \( +V_{\text{DC}} \) or \( -V_{\text{DC}} \). So, this circuit can be used a 2-level inverter as well.
b. SPTT Switch or a simple 3-level inverter realization

Fig. 6 depicts the electronic realization of Single Pole Triple Throw (SPTT) switch. It is observed that the waveform quality of such an SPTT switch is superior to that of a SPDT switch.

Case 1: In order to connect P” to T1, S1 and S2 must be ON.
Case 2: In order to connect P” to T2, S2 and S3 must be ON.
Case 3: In order to connect P” to T3, S3 and S4 must be ON.

The waveform quality of an SPTT switch is attributed due to the following reason. The average pole voltage at P” at any point will be the average of the voltages at T1, T2 and T3. If T1 is at +0.5V_{DC}, T3 at -0.5V_{DC} and T2 at 0V, then V_{P”} is between +0.5V_{DC} and -0.5V_{DC}. If we want to obtain a pole voltage of 0.25V_{DC}, we can realize it using a 2-level inverter. It can be obtained by applying +0.5 V_{DC} for a longer time and -0.5 V_{DC} for a relatively shorter time, so that the average of the voltage applied approximates to a 0.25 V_{DC}. However, the same realization can be done using a 3-level inverter as follows. A 3-level inverter, as the name suggests, can produce 3 output voltage levels: ±0.5 V_{DC} and 0. So, simply apply +0.5 V_{DC} and 0V for the same amounts of time. This second method is much more efficient and generates a waveform of better quality than that produced using a 2-level inverter, since it is a time-averaging technique and it ensures that the maximum instantaneous error possible. Yet another advantage of this method is that the diodes D1 and D2 keep a constant check to ensure that the switches only work between the specified voltage ranges [5], [6],[7].
B. TYPES OF MULTILEVEL INVERTERS

There are several major topologies of multilevel inverters that exist in literature; the classification is based on the different mechanisms involved. This paper discusses the types of symmetrical MLIs [5], [6], [7].

![Diagram of Multilevel Inverters]

**Fig. 7: The categories of multilevel inverters**

1. **Symmetrical Multilevel Inverters**
   These inverters have equal amplitude of voltage sources. Diode clamped (DMLI or neutral-point clamped), flying capacitor multilevel inverter (FCMLI or capacitor-clamped) [6] and Cascaded H-bridges converter (CMLI) (i.e., cascaded multicell using separate dc sources [1]) are the types of symmetrical multilevel inverters. H-bridge design was the first topology to be developed. In this, the scaling can be done easily. The H-bridge inverter consists of isolation transformers for isolating the voltage source. Then the diode-clamped inverter was developed. It consisted of a of a series capacitors. Later came the flying-capacitor topology. The difference compared to the diode-clamped inverter is that in flying-capacitor topology the voltage levels are clamped using floating capacitors [4].

   **Diode clamped or Neutral-point clamped (NPC) multilevel inverter**
   This inverter mainly uses diodes to limit voltage stress on the power device. Assume that the voltage across each capacitor and each switch is Voc. An m level inverter consists of (m-1) voltage sources, (m-1) capacitors, 2(m-1) switching devices and (m-1)*(m-2) diodes per leg [4], [8], [9].

   **Single-phase Three-level NPC Inverter**

![Diagram of Single-phase Three-level NPC Inverter]

**Fig.8: One leg of a 3-level NPC Inverter**
Case 1: To connect the pole P” to T1, S1 and S2 are ON, whereas S3 and S4 are OFF. Case 2: To connect the pole P” to T2, S2 and S3 are ON, whereas S1 and S4 are OFF. Case 3: To connect the pole P” to T3, S3 and S4 are ON, whereas S1 and S2 are OFF. So, we can see that S2 and S3 tend to ON longer than the switches S1 and S4, and consecutively dissipate more power than S1 and S4. So, the losses from S2 and S3 are higher than the losses from S1 and S4. So, we need two different gating signals— one for S1 and S3, and another for S2 and S4 (since these pairs are complementary during operation). So, comparison we find that a 2-level inverter requires only a single gating signal, whereas a 3-level inverter requires 2 gating signals.

b. **Flying capacitor multilevel inverter**
This inverter mainly uses capacitors to limit voltage stress on the power device. The circuit diagram is very similar to the diode-clamped multilevel inverter, with the only difference that capacitors are used to divide the input DC voltage, so that the voltage across each of the capacitors as well as each switch is V<sub>DC</sub>. For an m-level inverter, (m-1) capacitors are required. The diodes of the diode-clamped MLI are replaced by capacitors. However, at the input end, the 2 capacitors will be pre-charged to a fixed voltage level in order to act as the DC voltage source, whereas, the other two capacitors will not be connected to any fixed voltage—in other words it is varying and hence the name „flying“. The Fig. 9 shows the 5-level flying capacitor clamped MLI [8], [9], [10].

\[ \text{Fig. 9: 5-level flying capacitor clamped MLI} \]

\[ \text{c. Conventional Cascaded multilevel inverter} \]
This type of inverter is based on H-bridge inverters—they are connected together in series. The output voltage will be sinusoidal in nature. It is calculated as the sum of the voltages produced by each of the cells. If n is the number of cells, then there will be (2n+1) output voltage levels. The main plus point of the cascaded MLI is that it uses lesser number of component devices compared to the other two types of symmetrical MLIs. Thereby, the price as well as the weight of the cascaded MLI is comparatively much less than the other two types of MLI topologies [10], [11], [12].

i. **Single-phase Cascaded 3-level inverter realization**
The Figure below (Fig. 10) depicts a cascaded inverter with multiple levels.

\[ \text{Fig. 10: Conventional Cascaded 3-level MLI realization} \]
For switch Sn, the transistor is represented as Qn and the diode as Dn. The working of the circuit is as follows:

Case 1: Applying the gating signal, if switch S1 is ON, transistor Q1 and Q4 will be ON or diodes D2 and D3 will be ON. Then the output is $+V_{DC}$.

Case 2: If S2 is ON, Q2 and Q3 will be ON or D1 and D4 will be ON. The output is $-V_{DC}$.

Case 3: However, if S3 is ON, then either Q1 or D3 will be ON, or D1 and Q3 will be ON. In either case the output will be $V_{out} = 0V$.

Case 4: Similarly, if S4 is ON, then either Q2 or D4 will be ON, or D2 and Q4 will be ON. In either case the output will be $V_{out} = 0V$.

**C. FIVE-LEVEL MLI**

In a 2-level inverter, the output voltage can have only 2 voltage levels. A 3-level inverter in the other hand can have $\pm V_{dc}/2$, 0 (3 values). This section observes how the output voltage value changes for a 4-level and 5-level MLI [10], [11], [12], [13], [14]. The circuit shown in Fig. 11 is that of a single pole four throw switch which consists of one pole and 4 throws.

![Fig. 11: Single Pole Four Throw switch](image)

The pole voltage can take values: $\pm 0.5 \ V_{DC}$, $\pm 0.167 \ V_{DC}$.

The Fig. 12 depicts a single pole five throw switch.

![Fig. 12: Single Pole Five Throw switch](image)
The pole voltage can take values: ±0.5 VDC, ±0.25 VDC, 0.

**a. Single-phase Five-level NPC Inverter**

i. Diode-clamped inverter

Initially, to start with, let us consider a 5-level diode-clamped inverter. Take one leg first. The dc rail 0 is the reference point of the output phase voltage. The steps to obtain the 5-level waveform are:

Case 1:
For an output voltage level \( V_{out} = V_{DC} \), turn on all upper-half switches S1 through S4.

Case 2:
For an output voltage level \( V_{out} = V_{DC}/2 \), turn on two upper switches S3 through S4 and two lower switches S1” and S2”.

Case 3:
For an output voltage level \( V_{out} = 0 \), turn on all lower half switches S1” through S4”.

State 1 is known as ON condition whereas State 0 is known as OFF condition. Each switch is turned ON only for one unit time per cycle. The architecture in Fig. 5 consists of four complementary switch pairs in each phase.

![Fig. 13: Diode-clamped multilevel inverter with 5-levels](image)

The switch-pairs forming the inverter legs are (S1, S1”), (S2, S2”), (S3, S3”) and (S4, S4”). Therefore, if any one of the switch in the complementary pairs is ON, the other switch of the same pair must be OFF. The line voltage consists of the positive phase-leg voltage of terminal and the negative phase-leg voltage of terminal. Each phase-leg voltage tracks one-half of the sinusoidal waves. So, the resulting line voltage is a five-level staircase wave with reduced oscillations (refer Table 1 below).
TABLE 1

DIODE CLAMPED INVERTER -SWITCH STATES AND OUTPUT VOLTAGE LEVELS

<table>
<thead>
<tr>
<th>SWITCH STATE</th>
<th>S1</th>
<th>S2</th>
<th>S3</th>
<th>S4</th>
<th>S1”</th>
<th>S2”</th>
<th>S3”</th>
<th>S4”</th>
<th>OUTPUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>+ Vdc/2</td>
</tr>
<tr>
<td>OFF</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>+ Vdc/4</td>
</tr>
<tr>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>0</td>
</tr>
<tr>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>- Vdc/4</td>
</tr>
<tr>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>- Vdc/2</td>
</tr>
</tbody>
</table>

ii. Flying capacitor-clamped inverter

Fig. 14 shows the flying capacitors based multilevel inverter topology.

Fig.14: Flying capacitor multilevel inverter with 5-levels
A relative reduction in components is achieved, because fewer capacitors are required in the overall system. However, this is not the main objective of the proposed HMMC with benefits derived from the reduced capacitor voltage ripples as shown in table 2 the capacitor voltages. As the FC cell is connected across all three phases of the converter, the voltage oscillations cancel out between the three phases, reducing the voltage ripple to a minimum.

**FLYING CAPACITOR INVERTER-SWITCH STATES AND OUTPUT VOLTAGE LEVELS**

<table>
<thead>
<tr>
<th>SWITCH STATE</th>
<th>CAPACITOR STATE</th>
<th>OUTPUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>S1 S2 S3 S4</td>
<td>C3” C4” C5”</td>
<td>+ (V_{dc}/2)</td>
</tr>
<tr>
<td>ON ON ON ON</td>
<td>Not charging</td>
<td>Not charging</td>
</tr>
<tr>
<td>ON ON ON OFF</td>
<td>Not charging</td>
<td>+</td>
</tr>
<tr>
<td>ON ON OFF ON</td>
<td>Not charging</td>
<td>+</td>
</tr>
<tr>
<td>ON OFF ON ON</td>
<td>+</td>
<td>-</td>
</tr>
<tr>
<td>OFF ON ON ON</td>
<td>-</td>
<td>Not charging</td>
</tr>
<tr>
<td>OFF OFF ON ON</td>
<td>Not charging</td>
<td>Not charging</td>
</tr>
<tr>
<td>OFF ON OFF ON</td>
<td>-</td>
<td>+</td>
</tr>
<tr>
<td>OFF ON ON OFF</td>
<td>Not charging</td>
<td>+</td>
</tr>
<tr>
<td>OFF ON OFF OFF</td>
<td>-</td>
<td>Not charging</td>
</tr>
<tr>
<td>ON OFF OFF ON</td>
<td>+</td>
<td>-</td>
</tr>
<tr>
<td>ON OFF ON OFF</td>
<td>+</td>
<td>-</td>
</tr>
<tr>
<td>ON ON OFF OFF</td>
<td>Not charging</td>
<td>+</td>
</tr>
<tr>
<td>ON ON OFF OFF</td>
<td>Not charging</td>
<td>+</td>
</tr>
<tr>
<td>ON OFF OFF OFF</td>
<td>+</td>
<td>Not charging</td>
</tr>
</tbody>
</table>

*TABLE 2*
The DC-DC stage present between the ESS and the SM capacitors in MMC-based converters should operate in a manner so that the voltage at the ESS side is kept constant and without low-order harmonics. This task is simplified if the ESS is connected to the three-level FC-SM, as the voltage of the capacitor does not have low-order oscillations.

Single-phase Cascaded 5-level inverter realization

![Diagram](image)

Fig.15: Cascaded multilevel inverter with 5-levels

A second requirement for the operation of the MMC is balancing of the SM capacitor voltages, which can be implemented either with the use of sorting algorithms or by making use of the natural balancing property of phase-shifted pulse-width modulation (PS-PWM). In the case of the proposed HMMC, the capacitors of the FC SM will exhibit significantly lower voltage oscillations requiring modifications to the existing sorting algorithms.

### TABLE 3

| SWITCH STATES AND VOLTAGE LEVELS OF FIVE LEVEL CASCADED INVERTER |
|-------------------|-------------------|-------------------|
| SWITCH STATE      | OUTPUT (V<sub>dc</sub>) |
| S1 X S2 X         | S<sub>1</sub> X+1  | S<sub>2</sub> X+1  |
| ON OFF ON OFF     | +2 V<sub>dc</sub>  | + V<sub>dc</sub>  |
III. SIGNIFICANCE OF THE NUMBER OF LEVELS IN A MULTILEVEL INVERTER

A. Losses in 2-level inverter

The 3-phase Voltage-source inverter in Fig.4 has been represented in its electronic realization in the Figure below.

![Fig. 16: 2-level Voltage Source Inverter](image)

Here the losses in all the 3 legs are equal since it is a balanced load condition that we are considering. That implies that the losses due to bottom and top devices are the same. The losses include both the conduction and the switching losses. If PWM techniques are applied, however, this balance load condition may get varied and hence may lead to unequal losses in each leg.
B. Losses in 3-level inverters

This is not the same case in multilevel inverters with 3 or more levels - the working is different. Consider Fig. 10 before. As we said there that since switches S2 and S3 are ON for more time than S1 or S4, the power dissipation is higher in that case. That means in turn that the conduction losses are also higher in S2 and S3. Rather, the middle two devices suffer more losses [11], [12], [13], [14].

Conduction losses and harmonics:

\[ P_{\text{cond-S2}} = I_{S_{12}}^2 \times R_{DS} \]
\[ I_{S_{12}}^2 = D_2 \times \left[ \frac{I_{0} S_{12} + \Delta I_{0} S_{12}}{12} \right] \]
\[ \Delta I_{0} S_{12} = \frac{I_{0} S_{12} - \text{max} - I_{0} S_{12} - \text{min}}{2} \]

IV. THE PROPOSED NOVEL BRIDGED-INSERT CASCADED MLI

Considering the main disadvantage of the Cascaded MLI topologies, we find that the number of switches used for the circuit are much higher and hence account for a higher loss. Correspondingly even the harmonic distortion will be much higher. To overcome this problem, this paper propose a bridged-insert cascaded MLI topology. A 5-level MLI of this type is shown below:

![Fig. 17: Bridged-Insert Cascaded 5-level MLI](image)

As you can see, the number of switches has been reduced by 4 and hence the loss can also be reduced.

DIAGRAMATIC DESCRIPTION

The proposed topology consists of a bridge-like construction similar to that of an H-bridge. The diodes D_{bridge1}, D_{bridge2}, D_{bridge3} and D_{bridge4} form this section. The serial connection of D_{bridge1}, D_{bridge2} and D_{bridge3}, D_{bridge4} are connecting in parallel. The DC voltage \( V_{DC} \) is applied across the serial connection of \( D_{bridge1}, D_{bridge2} \) and across the serial connection of \( D_{bridge3}, D_{bridge4} \). The positive terminal of the DC voltage is applied at the n-side of \( D_{bridge1} \) and \( D_{bridge3} \), and the negative terminal of the DC voltage is connected to the p-side of \( D_{bridge2} \) and \( D_{bridge4} \). There are four switches used in the topology, marked as \( S_1, S_2, S_3 \) and \( S_4 \). Each switch consists of a parallel combination of an IGBT and a diode. As can be seen in figure, the switches \( S_1 \) and \( S_3 \), and \( S_2 \) and \( S_4 \) are series connected. The series combination of \( S_1-S_3 \) and \( S_2-S_4 \) are parallel connected. This section is connected across the junction of \( D_1-D_3 \) and \( D_2-D_4 \) in parallel, as a load of the H-bridge. The final stage load is connected across the junctions of \( S_1-S_3 \) and \( S_2-S_4 \). The voltage across the load is depicted as \( V_{out} \). \( V_{out} \) is the final five-stage MLI output, which can be approximated close to a sinusoidal or AC output.
OPERATIONAL DETAILS

As is known, a p-n junction diode has a junction voltage of 0.7V, which is required for turning ON the diode. In other words, it means that it is the voltage drop across the diode when it turns ON. A positive voltage applied at the p-side causes the diode to turn ON. A negative voltage applied at the p-side turns it OFF. When the DC voltage is positive, all the diodes D1, D2, D3 and D4 are OFF. This causes the voltage $V_{DC}$ to appear across the switch section. The positive voltage is at the lower end and negative at the upper end. This causes $S_3$ and $S_4$ to conduct and $S_1$ and $S_2$ to be OFF. When the DC voltage is negative, all the diodes D1, D2, D3 and D4 are ON, however on based on the voltage drops across them. The corresponding output across then is applied across the switch section also. Correspondingly, it this causes $S_3$ and $S_4$, and $S_1$ and $S_2$ to conduct. The working can be understood in the Table below that explain the devices that are ON and OFF and the corresponding output voltages.

### THE EPSO ALGORITHM

The Enhanced particle swarm algorithm begins by creating the initial particles, and assigning them initial velocities. It evaluates the objective function at each particle location, and determines the best (lowest) function value and the best location. It chooses new velocities, based on the current velocity, the particles' individual best locations, and the best locations of their neighbors. It then iteratively updates the particle locations (the new location is the old one plus the velocity, modified to keep particles within bounds), velocities, and neighbors. Iterations proceed until the algorithm reaches a stopping criterion. Here are the details of the steps. The algorithm here we proposed helps to obtain the best THD value.
The particle swarm paradigm is one of the latest population-based optimization methods, which does not use the filtering operation (such as crossover and/or mutation) and the members of the entire population are maintained through the search procedure. The EPSO algorithm is an adaptive algorithm based on a social psychological metaphor; a population of individuals (referred to as particles) adapts by returning stochastically toward previously successful regions. Particle Swarm has two primary operators: Velocity update and Position update. During each generation each particle is accelerated toward the particles previous best position and the global best position. At each iteration a new velocity value for each particle is calculated based on its current velocity, the distance from its previous best position, and the distance from the global best position. The new velocity
value is then used to calculate the next position of the particle in the search space. This process is then iterated for a set number of times, or until a minimum error is achieved.

EPSO PROGRAMMING DETAILS

<table>
<thead>
<tr>
<th>CONTENT</th>
<th>DATA</th>
</tr>
</thead>
<tbody>
<tr>
<td>POPULATION SIZE</td>
<td>20</td>
</tr>
<tr>
<td>PARAMETERS USED</td>
<td>X,V,a,m,s,Q,phi1,phi2,phi,xp,pdgtemp,</td>
</tr>
<tr>
<td></td>
<td>r4,k1,k2,k3,k4,k5,Vdc,vdc1,vdc2,vdc3,</td>
</tr>
<tr>
<td></td>
<td>vdc4,vdc5,gbestvar,gbest,tempo,pdg,pid</td>
</tr>
<tr>
<td>MAXIMUM ITERATION</td>
<td>50</td>
</tr>
<tr>
<td>NO. OF EXECUTION TIMES</td>
<td>30</td>
</tr>
<tr>
<td>VOLTAGES</td>
<td>Vdc=100v,Vdc1=108v,Vdc2=98v,</td>
</tr>
<tr>
<td></td>
<td>vdc3=90v,Vdc4=86v,Vdc5=80v,</td>
</tr>
<tr>
<td></td>
<td>Kn=vdcn/vdc</td>
</tr>
</tbody>
</table>

Particle swarm optimization (PSO) optimizes a problem by having a population of candidate solutions, here dubbed particles, and moving these particles around in the search-space according to simple mathematical formulae over the particle's position and velocity.

V. RESULTS AND DISCUSSIONS

The study and analysis of the diode clamped 5-level inverter, flying capacitor-clamped 5-level inverter, cascaded 5-level inverter as well as the proposed bridged-insert cascaded 5-level inverter were carried out using MATLAB/ Simulink Tool. The voltage output obtained across the load or in other words, at the pole was analyzed and compared. Not only that, the FFT (Fast Fourier Transform) analysis was also done in order to analyze the harmonic distortion present in the output. On comparison of the results obtained, it is evident that the proposed bridged-insert cascaded MLI is much more superior to the other discussed topologies when comparing the total harmonic distortion (THD) as well as the area usage.

a. Diode Clamped MLI
b. Flying-Capacitor Clamped MLI

Fig. 18: The output voltage waveform of the 5-level diode-clamped MLI

![Fig. 18](image1.png)

Fig. 19: The FFT of the 5-level diode-clamped MLI

![Fig. 19](image2.png)

Fig. 20: The output voltage waveform of the 5-level flying capacitor clamped MLI

![Fig. 20](image3.png)

Fig. 21: The FFT of the 5-level flying capacitor clamped MLI

![Fig. 21](image4.png)

c. Conventional Cascaded MLI

![Fig. 22](image5.png)
VI. ANALYSIS AND COMPARISON

The results from section V have been consolidated in this section using bar-chart. The Figures below show the comparison of the proposed bridged-insert cascaded MLI with diode-clamped, flying capacitor clamped and conventional cascaded MLI topologies in terms of the fundamental frequency, area coverage and THD as given in Table 5 below.

<table>
<thead>
<tr>
<th>TABLE 5</th>
</tr>
</thead>
<tbody>
<tr>
<td>RESULT SUMMARY</td>
</tr>
</tbody>
</table>

Caribbean Journal of Science
<table>
<thead>
<tr>
<th>Type</th>
<th>Fundamental in Hz</th>
<th>THD in %-age</th>
<th>Area (number of transistors)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Diode-clamped</td>
<td>38.7</td>
<td>21.97</td>
<td>8</td>
</tr>
<tr>
<td>Flying-Capacitor</td>
<td>967.4</td>
<td>39.92</td>
<td>8</td>
</tr>
<tr>
<td>Conventional</td>
<td>278.6</td>
<td>20.93</td>
<td>8</td>
</tr>
<tr>
<td>Cascaded</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Proposed</td>
<td>120</td>
<td>18.78</td>
<td>4</td>
</tr>
</tbody>
</table>

Diode-clamped vs Proposed- Fundamental frequency

Fig. 26: Fundamental Frequency comparison: Diode-clamped MLI vs Proposed

Fig. 27: THD comparison: Diode-clamped MLI vs Proposed
Flying-Capacitor clamped vs Proposed- THD comparison

Fig. 28: THD comparison: Flying-capacitor clamped MLI vs Proposed

Fig. 29: Fundamental Frequency comparison: Flying-capacitor clamped MLI vs Proposed

Fig. 30: Fundamental Frequency comparison: Conventional Cascaded MLI vs Proposed
Based on the analysis of the results given in this section, it can be seen that the proposed bridges-insert cascaded 5-level topology of MLI provides an area improvement of 50% compared to all other discussed topologies. The proposed design reduces the voltage oscillations by adapting the capacitor as auxiliary circuit, the fundamental frequency is a stable value at about 120Hz. The THD, on the other hand is improved by 10.27% compared to the cascaded topology, by 52.96% compared to flying capacitor clamped topology and by 14.52% compared to diode clamped topology. Hence, when you compared all the three parameters, we find that on the whole the proposed bridges-insert cascaded topology provides a better trade-off than the other topologies. Depending on the result obtained from the study conducted, a comparative analysis can be carried out. The above discussed types of MLI topologies are compared in a tabular format as shown below in Table 5 [11], [12], [13], [14]:

**TABLE 6**

<table>
<thead>
<tr>
<th>Type of MLI</th>
<th>Advantage</th>
<th>Disadvantage</th>
</tr>
</thead>
</table>
| Diode clamped multilevel inverter | 1. High efficiency.  
2. No need of filters for reducing harmonics.  
3. Reactive power flow can be altered.  
4. The control method is very simple. | 1. For high levels, more number of diodes are required.  
2. Real power flow control for individual converter is difficult. |
| Flying capacitor multilevel inverter | 1. Phase redundancies are available for balancing the voltage levels of the capacitors.  
2. The flow of Real and reactive power can be controlled.  
3. The large number of capacitors | 1. Control is complicated to track the voltage levels for all of the capacitors. Also, recharging all of the capacitors to the same voltage level is complex.  
2. Switching utilization and efficiency are poor for real power transmission.  
3. The large numbers of capacitors |
enables the inverter to ride through short duration outages and deep voltage sags.

are both more expensive and bulky than clamping diodes in multilevel diode-clamped converters. Packaging is also more difficult in inverters with a high number of levels.

**VII. CONCLUSION**

Depending on the comparative study made of the 3 types of symmetrical MLIs, it can be seen that the cascaded multilevel inverter requires minimum number of components when compared will other types, which thereby reduces the weight, price and size of the inverter device. With fewer switches or on-board components, the complexity of the circuit also reduces. So, it can be concluded that the proposed bridged-insert cascaded inverter is the better choice. However, if we are able to reduce the number of switches even further, the losses and harmonic distortions can be further comparatively reduced. Simulation Tests with this crane and control system showed that residual vibration can be reduced by an order of magnitude and can remain insensitive to large changes in payload location in the vertical direction. Hence, the novel topology of bridge-insert cascaded MLI was proposed. It used only 4 switches compared to the 8 switched used in the conventional cascaded MLIs, hence making the losses diminished. From the FFT analysis, it is found the harmonic distortions are also much reduced compared to the other inverter topologies. Hence the proposed technique of bridge-insert cascaded MLI is the best thanks to the help of proposed novel method and EPSO algorithm.

**REFERENCES**


